A study of source mask optimization for logic device through experiment and simulations

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ABSTRACT

Source and Mask co-Optimization (SMO) plays an increasingly important role in the advanced RETs required to continue shrinking designs in the low-k1 lithography regime. Instead of costly double pattering patterning techniques, SMO has been explored as an enabling technology for low-k1 design node. It is clear that intensive optimization of the fundamental degrees of freedom in the optical system allows for the creation of non-intuitive solutions in both the mask and the source, which leads to improved lithographic performance. In this work, source and mask shape for logic device have been optimized in order to improve process window of critical layouts which include complex 2D shape and dense contact. Tachyon SMO solution developed by BRION was introduced to obtain the optimization. In order to improve the accuracy of SMO model, AI blur which represents resist effect on wafer was considered during optimization. Based on simulation results, improvement in terms of process window as well as Mask Error Enhancement Factor (MEEF) was approximately 20 % in comparison with reference conditions. However, the corresponding experimental results should be investigated as the evidence of the performance SMO. These results demonstrate the importance of these considerations during optimization in achieving the best possible SMO results which can be applied successfully to the targeted lithography process.

Keywords: Lithography, Advanced RETs, Source Mask Optimization (SMO), Logic Device

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1. INTRODUCTION

As lithography moves further into the regime of low k1-factor, co-optimization of layout, mask, and lithography is critical to deliver a production-worthy patterning solution. The goal of co-optimization is to develop a design, along with it's RET (Resolution Enhancement Technology) solution that is less sensitive to manufacturing process variations. The most important performance metric of a given RET solution is its ability to deliver a specified depth of focus (DOF) and exposure latitude (EL), commonly referred to as process window (PW). For many years, the optimizations of the source topology and mask pattern correction [1, 2] have been developed in terms of theory rather than practical application because hardware was not able to support flexible illumination fully. Target function of source and mask optimization (SMO) is to define which value can be minimized by optimization of source and mask shape. In SMO, the input is basically a given clip containing the target design, and the output of the optimization consists of an illumination source shape together with a clip containing the corresponding OPC. As such, a routine for source optimization is not new, but the novelty mainly lies in the co-optimization of the mask, and the output of freeform sources. In freeform illumination, there is basically unlimited freedom in intensity and position of the light in the illumination pupil. In practice, a freeform source is often pixelated, with free choice of intensity per pixel, and smoothened by a point spread function. Similar to the traditional standard source shapes (e.g. Quasar, CQuad, Annular), freeform illumination shapes can be achieved on scanners using diffractive optical elements (DOE), which create one particular source shape. Additionally, a programmable illuminator called FlexRay™ is presented on ASML scanners as an option which allows instantaneous and unlimited variations of source shape set-up [3, 4]. The final goal of the SMO & freeform illumination technique is firstly to increase the yield of the lithographic process and increase process latitude or MEEF. In addition, the technique can create margin that allows for further downscaling of the device. In particular, SMO solution has been applied into LOGIC device which includes SRAM pattern [5, 6]. In terms of lithography, it is difficult that all types of SRAM shape can be patterned because it includes non-periodic and irregular shapes.

In this work, source and mask shape for logic device have been optimized in order to improve process window of critical layouts which include complex 2D shape and dense contact. Tachyon SMO solution which can provide full SMO procedure was introduced to obtain the optimization. In order to mimic real calibration model of SMO model, AI blur which represents resist effect on wafer was considered during optimization. In addition, control parameters such as weight of DOF, EL and MEEF should be tuned finely for the better results. Based on simulation results, improvement in terms of process window as well as Mask Error Enhancement Factor (MEEF)

was approximately 20 % in comparison with reference conditions. However, the corresponding experimental results should be investigated as the evidence of the performance SMO. These results demonstrate the importance of these considerations during optimization in achieving the best possible SMO results which can be applied successfully to the targeted lithography process.

2. SOURCE MASK OPTIMIZATION (SMO) flow

A novel SMO method that achieves simultaneous co-optimization of source and mask has been introduced in reference [7] This approach has been shown to offer significant process window improvements over earlier, iterative approaches, by generating first a fully unconstrained solution, then introduces realistic manufacturing constraints for either mask and source. Fully unconstrained here refers to an idealized, pixelated freeform source and a hypothetical continuous transmission mask (CTM) that are simultaneously co-optimized in order to define the ultimate PW entitlement for the given imaging problem. This co-optimization flow is schematically outlined in Fig.1, using the example of a typical contact pattern clip for illustration.

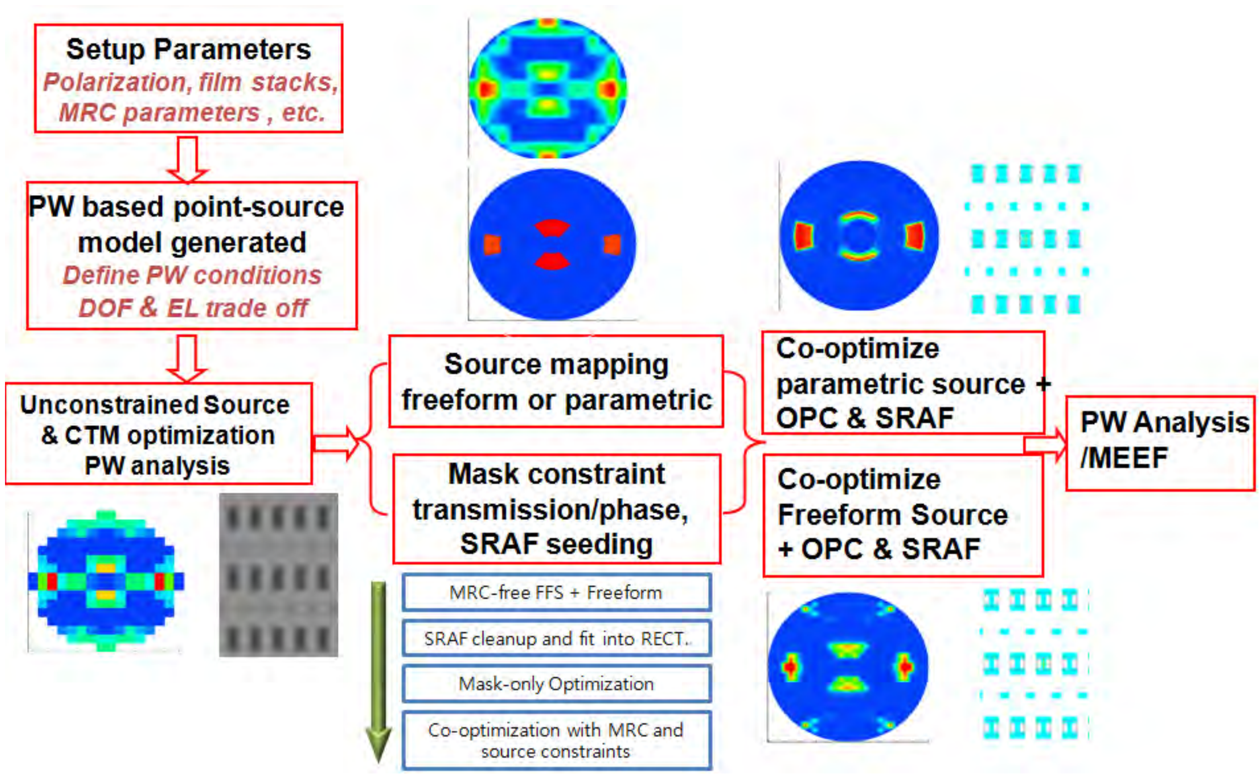

Fig 1. Source and mask co-optimization flow

The first step of the CTM/SMO job setup is to define all the input parameters for the optimization as schematically shown in Fig1, block a. These setup parameters are used throughout the entire flow, and the various constraints will determine later how the unconstrained freeform source will be converted and co-optimized. Another key input is the definition of process window conditions to be used in the optimization. Typically these will include defocus, dose conditions and mask bias in order to capture DOF, EL and MEEF performance and allow suitable weighting or trade-offs between these metrics as shown in Fig. 1, block b. With all the setup parameters, block c starts the co-optimization with unconstrained freeform source and continuous transmission mask using the point source models from the previous step. Without constraints, optimization in this stage will search for solutions in the largest possible solution space, and give the best possible process window and MEEF. It is shown in Fig. 1, block d and e. The unconstrained solution will provide a valuable assessment of the ultimate PW entitlement and clearly flag problems that are not solvable by SMO but must be addressed by design rule optimization. However, neither unconstrained source nor continuous transmission mask are actually manufacturable. The idealized source map needs to be converted into a manufacturable illuminator shape by considering manufacturing constraints by a predictive, physical illuminator model as well as user preferences, e.g. choice between different DOE types (Fig.1 f, g). After also fixing the mask to a fixed transmission value (Fig.1 block i) the selected source-mask combination is co-optimized using the scanner illuminator and mask manufacture rule check (MRC) constraints.

[Cost function and algorithm]

Other key aspects of the Tachyon SMO application are the optimization algorithm, PW sampling strategy and the cost function. The algorithm will optimize the most intuitive measure of pattern printing fidelity, i.e. edge –or, resist contour-- placement error (EPE) with respect to the target layout. As the optimization will cover multiple process window conditions, including focus, dose and mask bias variation, the optimization is sensitive to DOF, EL and MEEF as well as underlying, related parameters such as NILS which e.g. directly corresponds to the variation of EPE with dose.

The cost function is conceptually defined as:

$$CF = \min_{pw} \max_{x} w(pw, x) \left\| \mathrm{EPE}(pw, x) \right\| \tag{1}$$

Where a computationally efficient implementation of the minmax algorithm is achieved by minimizing the sum of EPEs by using an LP norm as discussed in ref. [7]:

$$CF = \sum_{pw} \sum_{x} w(pw, x) \left\| \mathrm{EPE}(pw, x) \right\|^{p} \tag{2}$$

In either case, CF is the cost function, PW covers the user specified focus and dose range and mask bias for optimization, while x refers to a set of evaluation points on the target layout, where distance to the simulated resist contour is determined.

The objective of the minimax optimization algorithm is to minimize the worst case EPE, across all PW conditions, which will effectively stabilize the most variation-sensitive features. The user –definable weighting factors w(pw,x) provide flexibility to adjust relative significance of each sampling point, and allow to fine tune the SMO results and achieve possible trade-offs between the different success n metrics, such as MEEF and DOF. The cost function in Eq.1 is directly linked to a physical quantity related to critical dimension (CD). It naturally covers objectives from other common choices of cost function that correlates to the image merit function. For example, minimizing the EPE through dose is equivalent maximizing NILS at contour edges. This is achieved by including two dose settings in process window conditions. Mask error factor (MEF) is one of the most critical parameters that need to be considered in the optimization. The EPE cost function can directly incorporate mask error as a third dimension to the conventional focus-exposure process window optimization.

3. APPLICATION OF SMO FOR LOGIC DEVICE

In SMO procedure, it is critical that target layouts and gauge line were defined because cost function optimizes edge placement error along the gauge line which engineer defines. Figure 2 shows target layouts which consist of one clear tone and two dark tones for this study. All layouts come from 2X SRAM layout where we suffer from lack of process margin such as depth of focus. Clear 1 mask includes periodic one dimensional pattern and complex two-dimensional pattern. In general, it is difficult to determine source for combination of 1-D and 2-D pattern. Two dark tone masks also were chosen as SMO target because dense contact layout near pitch limitation under ArF source usually has small process margin. SEM images in Figure 2 are pattern on the wafer at the best condition.

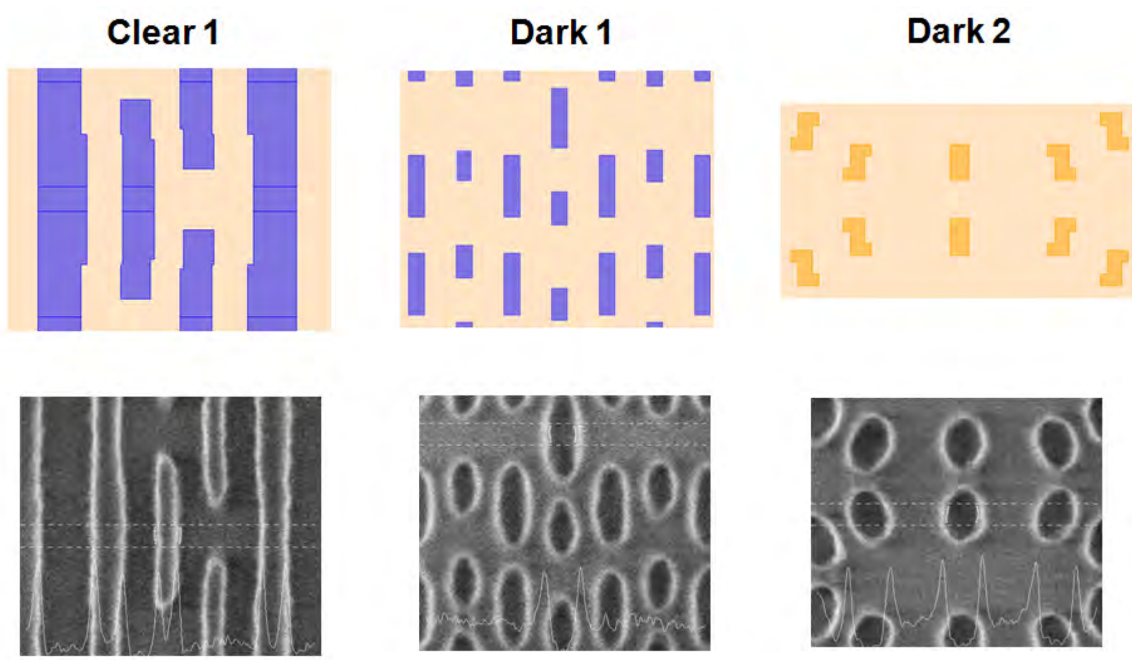

Fig 2. Target layouts for SMO

Gauge lines of each layout also are established in critical dimension. Before the SMO procedure starts, N.A. and polarization are 1.35 and TE, respectively. Only Binary mask is considered for this study.

As SMO preparation, OPC parameters such as minimum size of jog, MRC conditions and so on also were dealt with. In order to obtain practical intensity threshold, anchor pattern was used for each case. Furthermore, process window evaluation conditions are as follows; defocus: +/- 40nm, delta Dose: +/- 3%, mask bias: +/- 0.5nm (per edge). However, weight factors for each PW value such as defocus, delta dose and mask bias were tuned finely so as to obtain the better process window. In case of SRAF type, nominal generation rule of SRAF was introduced even though SRAF conditions affect OPC results like process window and edge placement error. In addition, AI blur factor was considered as 10 nm which was well-known as common value based on experience.

With the setup parameters, SMO results for cell1 were obtained as shown in Figure 3. All cases with freeform source shows the best performance and were improved around 20 % in terms of process window compared with POR results.

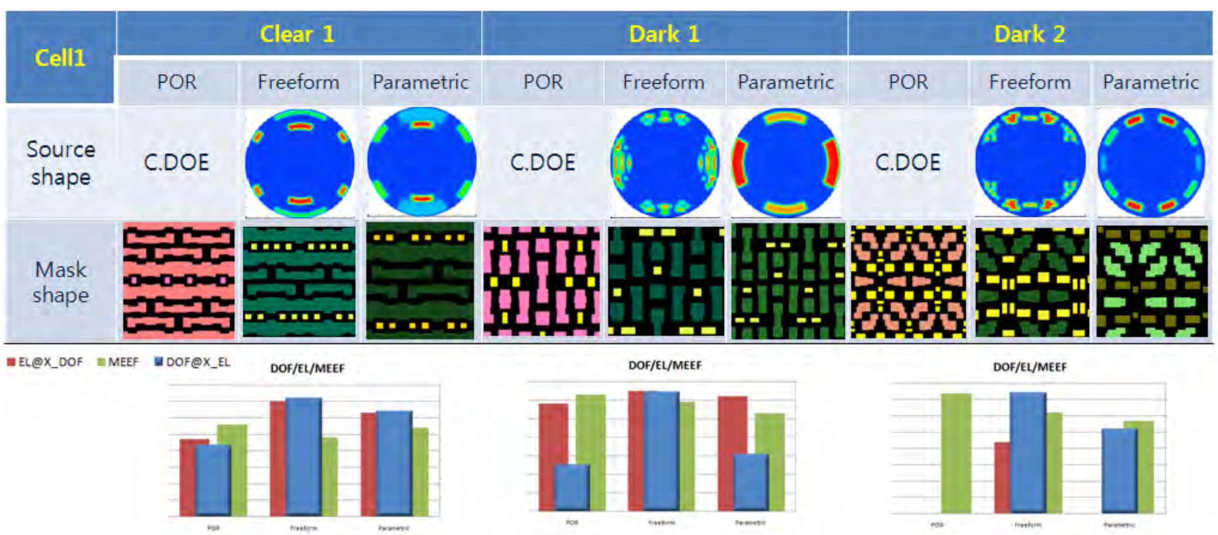

Fig 3. SMO results for cell_1

In order to demonstrate AI blur effect on simulation, source and mask results were calculated against AI blur value as shown in Figure 4. As our expectation, large AI value diminish process window of each case. However, proper AI value should be considered in order to improve model accuracy.

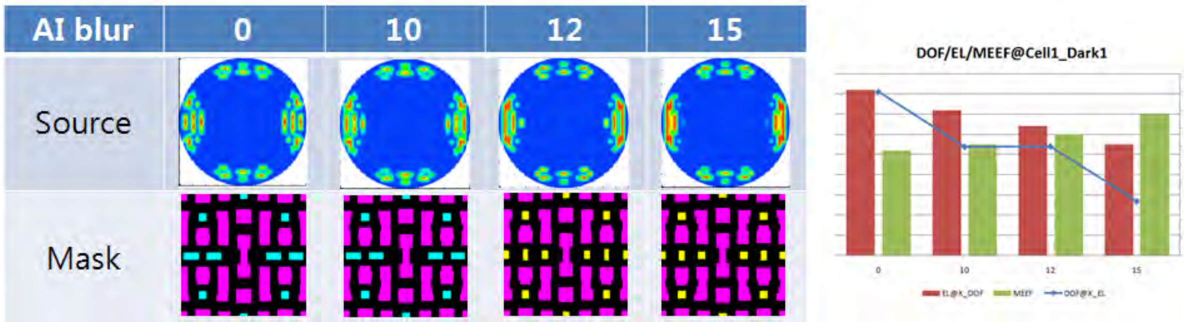

Fig 4. AI blur effect

All SMO results were inserted into mask which was taped out. Figure 5 shows mask image of SMO results where maximum process window was expected. Mean to target of Mask CD through the pitch also meets the specification.

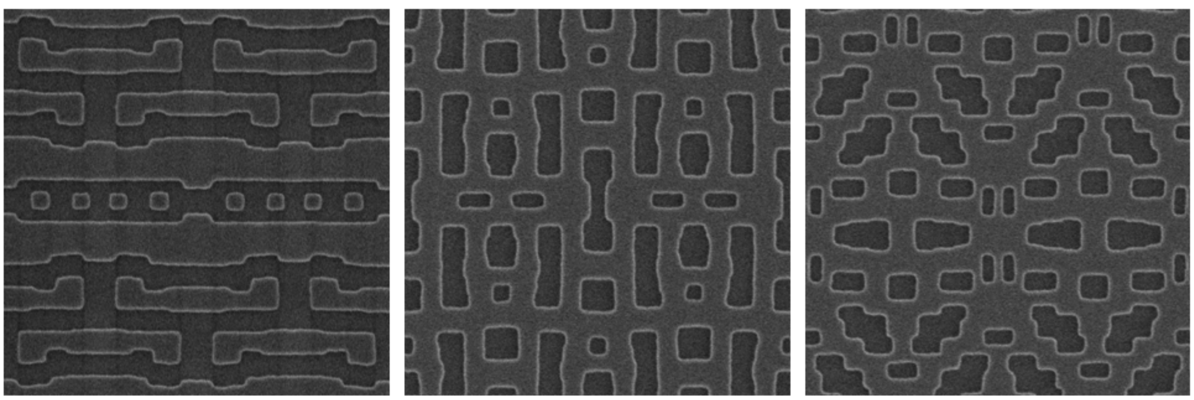

Fig 5. Mask image of SMO results

The mask will be evaluated by exposure under freeform source which Tachyon provided. Simulation and experiment results will be compared to verify SMO procedure. As well as, experimental results are able to tell us how to obtain accurate results.

4. CONCLUSION

Source and Mask co-Optimization (SMO) plays an increasingly important role in the advanced RETs required to continue shrinking designs in the low-k1 lithography regime. It is clear that

intensive optimization of the fundamental degrees of freedom in the optical system allows for the creation of non-intuitive solutions in both the mask and the source, which leads to improved lithographic performance. In this work, source and mask shape for logic device have been optimized in order to improve process window of critical layouts which include complex 2D shape and dense contact. Tachyon SMO solution developed by BRION was introduced to obtain the optimization. In order to improve the accuracy of SMO model, AI blur which represents resist effect on wafer was considered during optimization. Based on simulation results, improvement in terms of process window as well as Mask Error Enhancement Factor (MEEF) was approximately 20 % in comparison with reference conditions. However, the corresponding experimental results should be investigated as the evidence of the performance SMO. These results demonstrate the importance of these considerations during optimization in achieving the best possible SMO results which can be applied successfully to the targeted lithography process.

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